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A - 2851

Reg. No.:

Sixth Semester B.Tech. Degree Examination, May 2016 (2008 Scheme)

Branch : Electrical and Electronics

08.602 : MICROPROCESSORS AND APPLICATIONS

Time: 3 Hours

Max. Marks: 100

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Answer all questions. Each question carries 4 marks.

- 1. Explain the register structure of 8085.
- Explain the requirement of program counter, stack pointer and status flags in 8085.
- 3. Explain subroutine CALL and RET instructions in 8085.
- 4. Explain the common debugging methods.
- 5. How is memory interfacing done in 8085?
- 6. Explain the generation of control signals for memory and I/O devices in 8085.
- 7. Explain DMA data transfer scheme in 8085.
- 8. Explain the process of pipelining in 8086.
- 9. Explain the signals in 8086 specific for maximum mode.
- 10. Explain with examples string instructions of 8086.





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	PART-B	paFi
	Module – I	
11.	Draw and explain the internal architecture of 8085.	20
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12.	a) Draw the timing diagram of opcode fetch cycle of 8085.	10
	b) Write an 8085 ALP to sort an array in ascending order and descending order.	10
	Module – II	
13.	Explain the modes of operation of PPI 8255.	20
	OR	
14.	Explain interrupt structure of 8085 and interrupt driven data transfer.	20
10	swerall questions. Each question = sluboMarks.	
15.	Explain with timing diagram the minimum and maximum modes of operation of 8086. OR	20
16.	Explain the assembler directives for 8086 microprocessor. Bootem eniggudeb nommos ert nisigx 3	20
	How is memory interfacing done in 8085.?	
	Explain the generation of control signals for memory and I/O devices in 8085.	
	Explain DMA deta transfer scheme in 8085	
	Explain the process of pipelining in 8086.	8
	Explain the signals in 8086 specific for maximum mode.	